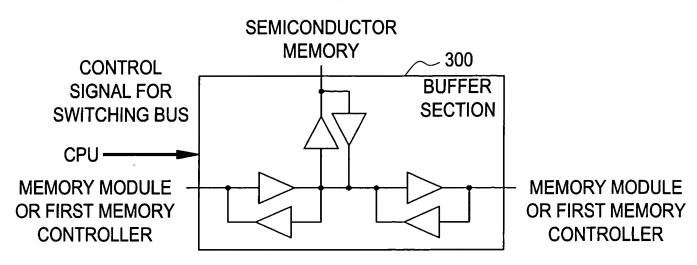
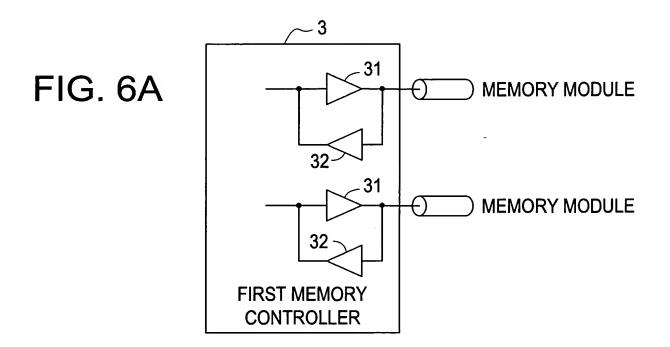


FIG. 5





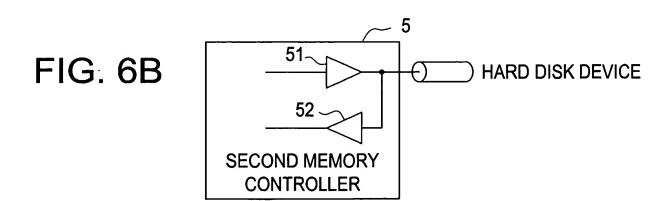


FIG. 8

MEMORY MODULE MEMORY BUFFER **BI-DIRECTIONAL BUS BI-DIRECTIONAL BUS** MODULE MEMORY MEMORY BUFFER MODULE MEMORY MEMORY BUFFER FIG. 10 **BI-DIRECTIONAL BUS** HARD DISK DEVICE MODULE MEMORY MEMORY BUFFER FIRST MEMORY CONTROLLER SECOND MEMORY CONTROLLER CPU GRAPHICS MEMORY

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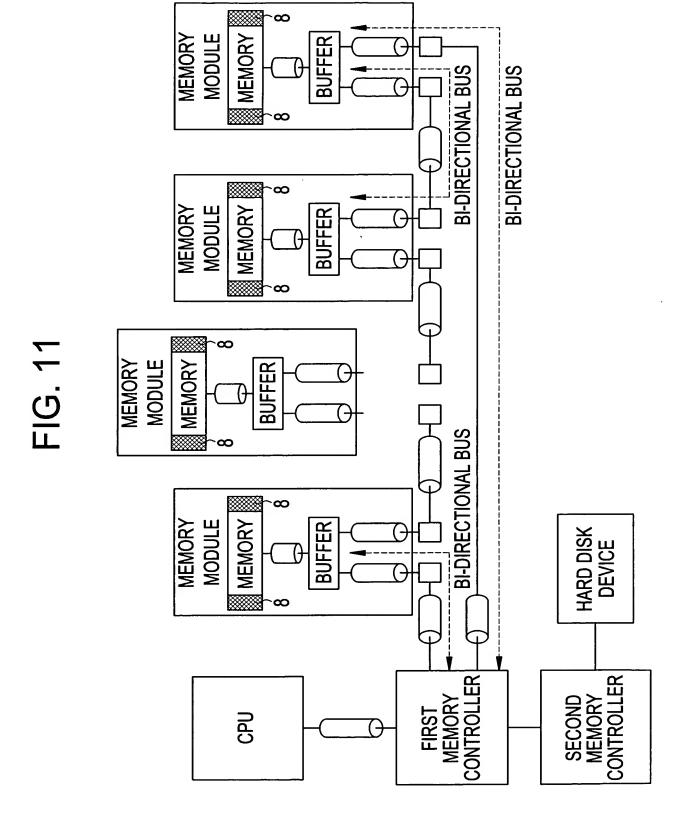


FIG. 13A

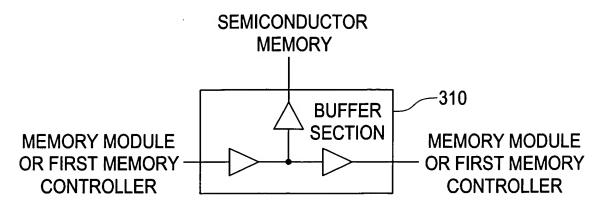


FIG. 13B

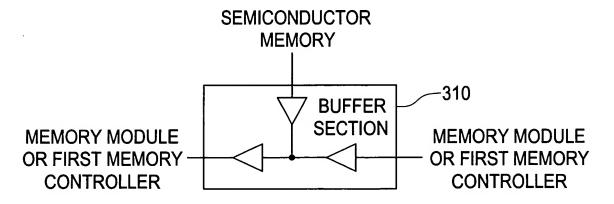


FIG. 14

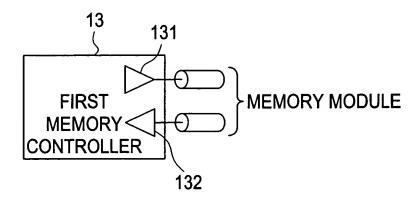


FIG. 15

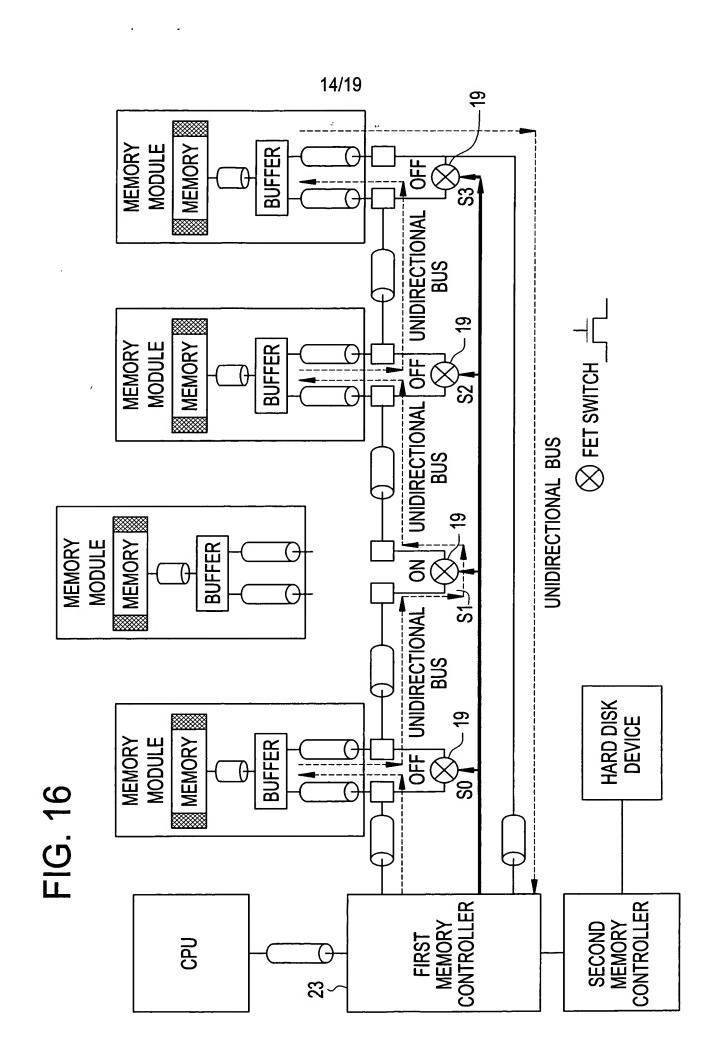
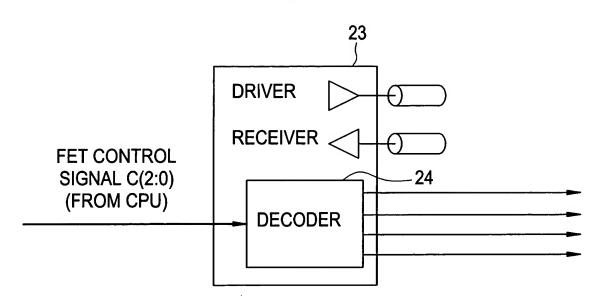


FIG. 17

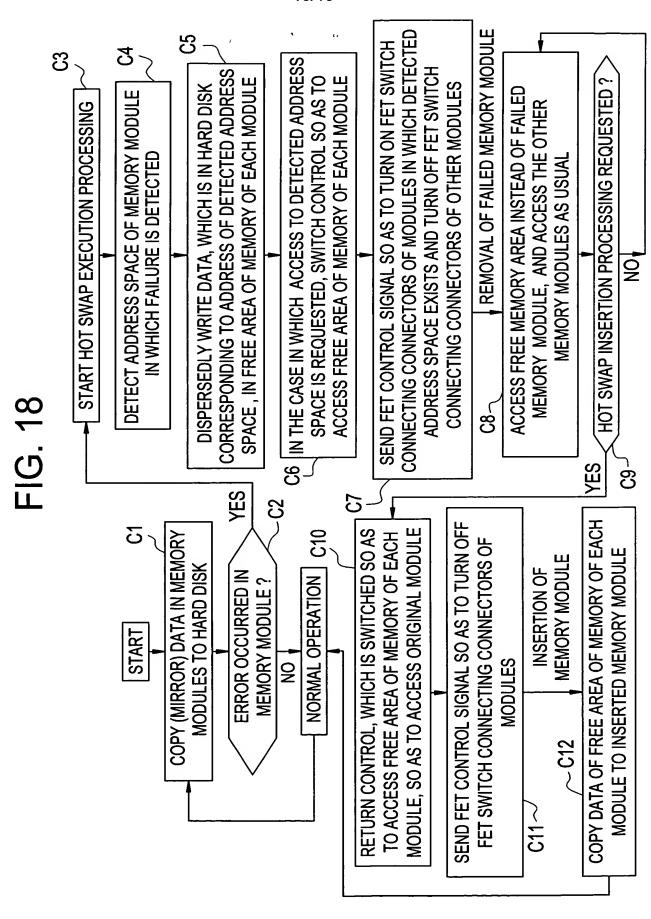


FET CONTROL SIGNAL						
C2	C1	C0	S3	S2	S1	S0
Н	Ш	Ш	L	L	L	L
L	L	L	L	L	L	Η
L	L	Н	L	L	H	لــ
L	Н	L	L	Н	L	L
L	Н	Ή	Н	L	L	L

L : FET SWITCH OFF

H: FET SWITCH

ON



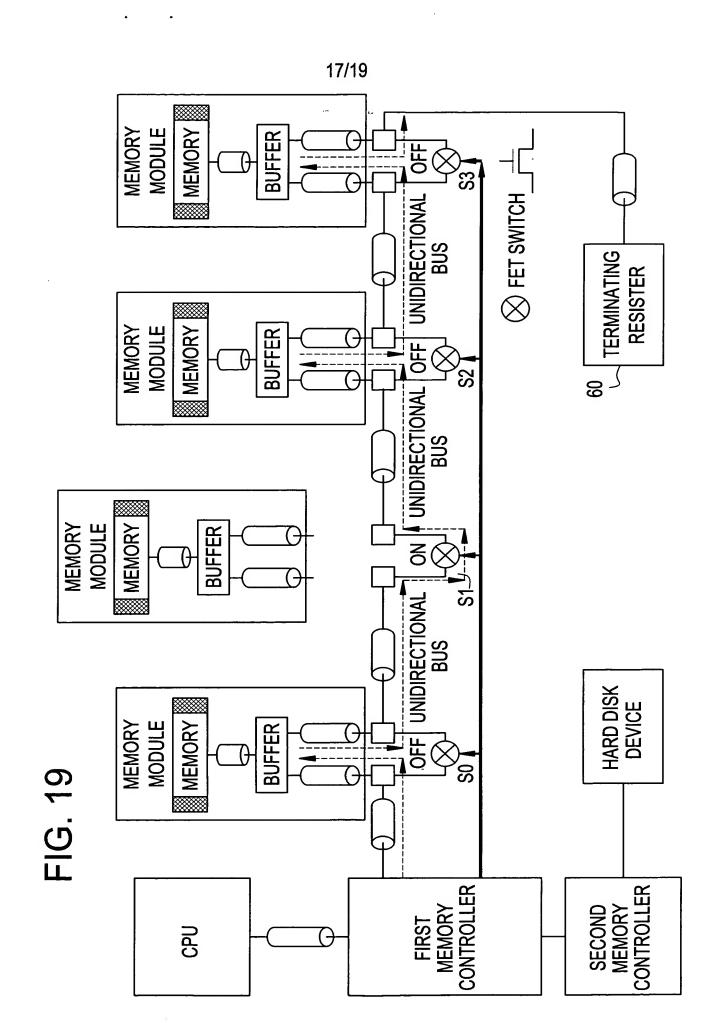


FIG. 20

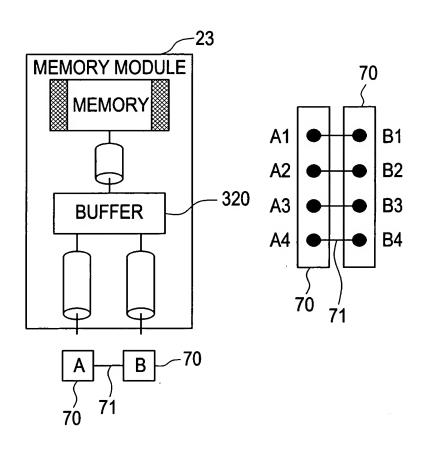


FIG. 21A

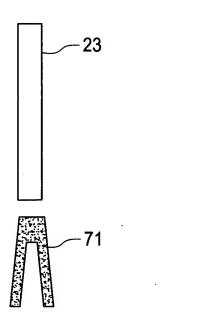


FIG. 21B

